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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,486	10/27/2003	Derryl D.J. Allman	01-689	4290
24319	7590	01/11/2006	EXAMINER	
LSI LOGIC CORPORATION 1621 BARBER LANE MS: D-106 MILPITAS, CA 95035			MITCHELL, JAMES M	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/694,486

Applicant(s)

ALLMAN ET AL.

Examiner

James M. Mitchell

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 November 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-9 and 19-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-9 and 19-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to the request for reconsideration filed November 2, 2005.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 4, 5, 8, 9, 19 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Saran (U.S. 6,625,882).

4. Saran (Fig.1, 2, 3, 4A,B) discloses:

(cl. 1, 8, 19, 23) a bonding pad for an integrated circuit the bonding pad comprising: a conductive base layer (80; Col. 5, Lines 15-17) having slots (e.g. spaces formed between multiple layers), the slots extending completely through the conductive base layer (Fig. 1), an insulating layer disposed on top of the conductive base layer (32, 34, 36), the insulating layer protruding into the slots of the conductive base layer, and the insulating layer including a low k material (col. 4, Lines 10-14), wherein the insulating layer comprises a base oxide layer (32) on top of the conductive base layer a low k dielectric layer (34) on top of the base oxide layer, and a cap oxide layer (36) between the low k dielectric layer and the conductive top layer (72), and a conductive top layer

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(76) disposed on top of the insulating layer, where the conductive base layer and the conductive top layer are not directly physically contacting one another (Fig. 1);

(cl. 4) and the base and top layer is aluminum (Col. 3, Line 6; Col. 5, Lines 15-19);

(cl. 5) and parallel slots (Fig. 2, 7);

(cl. 9) an integrated circuit (Col. 4, Lines 25-26).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 6, 7, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saran (U.S. 6,625,882).

8. Saran discloses the elements stated in paragraph 4 of this office action, but does not appear to explicitly disclose the thickness of the insulating layer form three to fifteen thousand angstroms.

9. However, applicant has not disclosed that the claimed thicknesses of the insulating layer was for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. As such, the claimed thickness would have been obvious, because applicant did not disclose that thickness of the insulating layer was for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

10. Claims 1, 2, 5-9 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiki et al. (U.S. 5,736,791) in combination with Saran (U.S. 6,625,882).

11. Fujiki (Fig. 1-3) discloses:

(cl. 1, 19) a bonding pad for an integrated circuit, the bonding pad comprising: a conductive base layer (3) having slots (13) formed therein the slots extending completely through the conductive base layer, an insulating layer (4) disposed on top of the conductive base layer, the insulating layer protruding into the slots of the conductive base layer, and

a conductive top layer (6) disposed on top of the insulating layer where the conductive base layer and the conductive top layer are not directly physically contacting one another (i.e. intermediate item 5);

(cl. 2) a plurality of vias (5) extending through the insulating layer and electrically connecting the base layer to the top layer;

(cl. 4) wherein the base and top layer is aluminum (Col. 9, Line 14, 33);

(cl. 5) wherein the slots of the conductive base comprise a pattern of substantially parallel slots (Fig. 1);

(cl. 6) wherein the slots of the base have a width of about eleven microns and a spacing of about three microns (Col. 9-10, Lines 66-5);

(cl. 7) with the insulating layer having a thickness (i.e. area via., 5 in);

(cl. 8, 23) multiple layers of the conductive base and the overlying insulating layer below the conductive top layer (Fig. 2);

(cl. 9) a bonding pad (also item 6; shown as a pad in Fig. 3).

12. With respect to claims 1 and 19, Fujiki does not appear to explicitly disclose that its insulating material layer comprises a base oxide on top of the base, a low k dielectric

on top of the base oxide, and a cap layer between the low k and conductive top layer, or that the thickness of the insulating layer form three to fifteen thousand angstroms.

13. Saran (Col. 4, Lines 10-14) utilizes comprises an insulating layer comprising a base oxide (32), a low k dielectric (34) on top of the base oxide, and a cap layer (36) between the low k and conductive top layer (72).

14. It would have been obvious to one of ordinary skill in the art to form the insulating layer of Fujiki with multiple layers of Saran that incorporates a low dielectric material, in order to increase circuit speeds and provide a reinforced structure as taught by Saran (Abstract; Col. 1, Lines 59-61).

15. Furthermore with respect to the thickness limitation of claims 6, 7, 21 and 22, applicant has not disclosed that the claimed thicknesses of the insulating layer was for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. As such, the claimed thickness would have been obvious, because applicant did not disclose that thickness of the insulating layer was for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

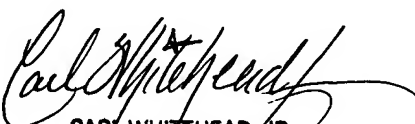
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jmm
December 28, 2005


CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
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